(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 089 344 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
04.04.2001 Bulletin 2001/14

(51) Int. Cl.[7]: **H01L 29/78**, H01L 21/336, H01L 29/51, H01L 21/28

(21) Application number: **00307920.9**

(22) Date of filing: **13.09.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **29.09.1999 JP 27625999**

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(54) Insulated gate field effect transistor and method of fabricating the same

(57) A field-effect transistor comprises a semiconductor substrate (101), a gate insulation film (111, 109') formed selectively on the semiconductor substrate (101), a gate electrode (106) formed on the gate insulation film (111, 109'), source/drain regions (107) formed in surface portions of the semiconductor substrate (101) along mutually opposed side surfaces of the gate electrode (106), the source/drain regions (107) having opposed end portions located immediately below the gate electrode (106), each of the opposed end portions having an overlapping region which overlaps the gate electrode (106), and a channel region (104) formed in a surface portion of the semiconductor substrate (101), which is sandwiched between the opposed source/drain regions (107). That portion (109') of the gate insulation film (111, 109'), which is located at the overlapping region where at least one of the source/drain regions (107) overlaps the gate electrode (106), has a lower dielectric constant than that portion (111) of the gate insulation film (111, 109'), which is located on the channel region (104). Thereby, a short channel effect can be fully suppressed, and a high-speed operation can be realized.

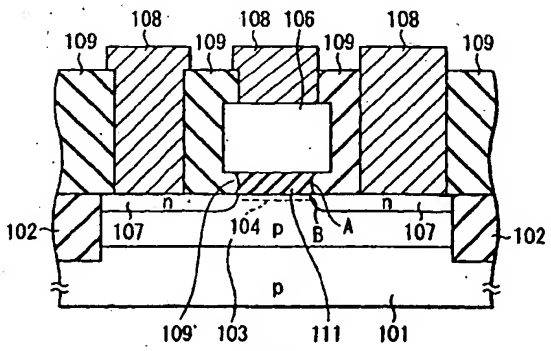

FIG. 4

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source/drain regions having opposed end portions located immediately below the gate electrode, each of the opposed end portions having an overlapping region which overlaps the gate electrode.

[0009] According to a third aspect of the invention, there is provided a method of fabricating a field-effect transistor, the method comprising the steps of:

forming a gate electrode over a semiconductor substrate, with a gate insulation film interposed therebetween;
forming source/drain regions in surface portions of the semiconductor substrate in a self-alignment manner with the gate electrode;
removing a portion of the gate insulation film from at least one side of the gate insulation film; and
forming a gate insulation region, which has a lower dielectric constant than the gate insulation film, at a region from which the portion of the gate insulation film is removed.

[0010] According to a fourth aspect of the invention, there is provided a method of fabricating a field-effect transistor, the method comprising the steps of:

forming a gate electrode over a semiconductor substrate, with a gate insulation film interposed therebetween;
forming a conductor film selectively on a side surface of the gate electrode;
forming source/drain regions in surface portions of the semiconductor substrate in a self-alignment manner with the gate electrode including the conductor film; and
a step of forming a gate insulation region, which has a lower dielectric constant than the gate insulation film, at a region between the conductor film and the substrate.

[0011] In the present invention, it is preferable that the dielectric constant of the gate insulation film on the channel region be set to be higher than that of a commonly used silicon oxide film. Examples of such a gate insulation film are a titanium oxide film, a silicon nitride film, a silicon oxynitride film, a tantalum pentoxide film, zirconium oxide film, hafnium oxide film, lanthanum oxide film, aluminum oxide film yttrium oxide film, scandium oxide film and a layered/mixed film of the foregoings. If the gate insulation film with such a high dielectric constant is used, the short channel effect can be effectively suppressed and the high current drivability can be realized. In addition, in the present invention, the dielectric constant of the gate insulation film on the source region and drain region is set to be lower than that of the gate insulation film on the channel region. Therefore, the parasitic capacitance is also reduced. As a result, the short channel effect can be effectively suppressed and the high-speed operation can be realized.

[0012] In addition, by creating a void in the gate insulation film on the source region or drain region, the capacitance between the source/drain region and the gate electrode can be further reduced. As a result, the short channel effect can be more effectively suppressed and the high-speed operation can be realized more effectively.

[0013] A description will now be given of the advantageous effect by which an increase in parasitic capacitance can be suppressed also by using the high-dielectric constant film as in the present invention.

[0014] FIG. 2 is a graph showing the dependency of the parasitic capacitance per unit width (a value obtained by subtracting the gate capacitance (created between the gate and channel) from the total load capacitance) upon the dielectric constant of the gate insulation film in the structure of the present invention and the prior-art structure. A curve marked by ○ indicates a dielectric constant in a case where the insulation film under the gate is uniform (FIG. 3A), and a curve marked by △ indicates a case where the dielectric constant of the insulation film under the gate is high only on the channel, and the dielectric constant on the source/drain is 3.9 (FIG. 3B). In either case, the abscissa indicates the dielectric constant of the gate insulation film on the channel and the ordinate indicates the parasitic capacitance per unit gate width.

[0015] In FIGS. 3A and 3B, the parameters of the devices are set as follows:

the gate length = 50 nm
the length of overlapping portion between the gate and the source/drain = 7 nm
the thickness of the gate insulation film = 1.5 nm × the dielectric constant of the high-dielectric constant film / 3.9
the impurity concentration of the well = 1×10^{18} cm^{-3}

[0016] FIG. 2 shows that the parasitic capacitance indicated by △ is decreased about 30% to 40%, compared to that indicated by ○. In the devices according to these examples, the gate capacitance is about 1 fF/μm, and the total load capacitance in the case indicated by △ is decreased about 10% to 20%, compared to the case indicated by ○. Taking into account the fact that the delay time is proportional to the load capacitance, the delay time in the structure shown in FIG. 3B decreases by about 10% to 20%, compared to the structure shown in FIG. 3A. In other words, a higher-speed operation can be performed with the structure according to the case indicated by △.

[0017] This summary of the invention does not necessarily describe all necessary features so that the invention may also be a sub-combination of these described features.

[0018] The invention can be more fully understood

region 103 is formed.

[0026] Then, as shown in FIG. 5B, for example, B ions are implanted in the p-well region 103 under conditions of 30 keV and 1.0×10^{13} cm^{-2} in order to obtain a desired threshold voltage. Thus, the impurity concentration of a near-surface portion of a channel region 104 is controlled.

[0027] In a subsequent step illustrated in FIG. 5C, a TiO_2 film 111 with a thickness of 15 nm, which will become a first gate insulation film, is formed by a process such as CVD (chemical vapor deposition).

[0028] In FIG. 5D, a polysilicon film 200 nm thick is deposited on the TiO_2 film 111 by LPCVD (low-pressure chemical vapor deposition). The polysilicon film is etched by an anisotropic etching process such as RIE (reactive ion etching), thus forming a gate electrode 106. The TiO_2 film 111, too, is subjected to anisotropic etching.

[0029] In the next step illustrated in FIG. 5E, for example, As ions are implanted under conditions of 50 keV and 5.0×10^{15} cm^{-2}, and the resultant structure is subjected to heat treatment. Thus, source/drain regions 107 are formed.

[0030] In FIG. 5F, the TiO_2 film 111 is subjected to isotropic etching such as CDE chemical dry etching so that a portion of the TiO_2 film 111, which lies on the source/drain region 107, may be removed.

[0031] Next, as shown in FIG. 5G, a silicon oxide film 109 with a thickness of 500 nm serving as an interlayer insulation film, is deposited by CVD, and contact holes 112 are formed by RIE on the source/drain regions 107 and gate electrode 106. In this step, the silicon oxide film 109 is made to fill the space created by the removal of the portion of the TiO_2 film 111.

[0032] Subsequently, an Al film 300 nm thick containing 1% of, e.g. Si is formed over the entire surface of the silicon substrate 101 by a process such as sputtering. The Al film is subjected to anisotropic etching such as RIE, and wiring 108 is formed. Thus, a filed-effect transistor having the structure as shown in FIG. 4 is fabricated.

[0033] The present invention is also applicable to cases where field-effect transistors are formed as part of semiconductor devices which include active devices such as bipolar transistors or single-electron transistors, or passive devices such as resistors, diodes, inductors or capacitors, in addition to field-effect transistors. Moreover, this invention is similarly applicable to SOI (silicon on insulator) devices.

[0034] In the first embodiment, As is used as impurities for forming the n-type semiconductor layer and B (boron) is used as impurities for forming the p-type semiconductor layer. It is possible, however, to use another Group V element as impurities for forming the n-type semiconductor layer and another Group III element as impurities for forming the p-type semiconductor layer. Besides, Group III impurities and Group V impurities may be introduced in the form of compounds containing them.

[0035] In the first embodiment, impurities are introduced by ion implantation. However, impurities may be introduced by other processes such as solid phase diffusion or vapor phase diffusion. In addition, a semiconductor containing impurities may be deposited or grown.

[0036] In the first embodiment, the device has the single drain structure. However, the device may have some other structure such as an LDD (lightly doped drain) or GDD (graded diffused drain) structure. Moreover, the device may have a pocket structure or an elevated source structure.

[0037] In the first embodiment, impurities are introduced in the source/drain regions 7 prior to the formation of the gate electrode 106 or gate insulation film 109'. However, the order of these steps is not essential and it may be reversed.

[0038] In the first embodiment, a silicide structure is not mentioned. It is possible, however, to adopt a suicide structure for the source/drain region 107 or gate electrode 106. Besides, it is possible to adopt of method of depositing or growing a metal layer on the source/drain regions 107.

[0039] In the first embodiment, the metal layer for wiring is formed by sputtering. The metal layer, however, may be formed by another method such as a deposition method. Furthermore, a method such as selective growth of metal may be adopted.

[0040] In the first embodiment, introduction of impurities in the gate electrode 106 is performed at the same time as the implantation of impurities for forming the source/drain. However, the impurities may be introduced in the gate electrode 106 in a step different from the step of introducing impurities for forming the source/drain. The method of introducing impurities in the gate electrode 106 is not limited to the ion implantation adopted in the first embodiment. It is also possible to introduce impurities by solid phase diffusion or vapor phase diffusion, or to form a silicon film containing impurities.

[0041] In the first embodiment, polysilicon is used for the gate electrode 106. However, the gate electrode 106 may be formed of single-crystal silicon, amorphous silicon, a metal, a metal-containing compound, or a lamination thereof. Although an upper part of the gate electrode 106 has such a structure that polysilicon is exposed, an insulator such as silicon oxide or silicon nitride may be provided on the upper part.

[0042] In the first embodiment, the gate electrode 106 is formed by anisotropic etching after the gate electrode material is deposited. However, the gate electrode 106 may be formed by using a burying process such as a damascene process.

[0043] In the first embodiment, the TiO_2 film formed by deposition is used as the first gate insulation film 111. However, another insulator film such as a nitride film, an oxynitride film, or a lamination film may be used. Moreover, some other high-dielectric constant film such

dielectric constant material. Moreover, as is shown in FIG. 10, the high-dielectric constant gate insulation film 111 may be formed in a tailing fashion so that both the uppermost portion of the substrate and the lowermost portion of the gate electrode 106 may be covered with the high-dielectric constant material. In order to suppress the capacitance created between the source/drain region 107 and the gate electrode 106, however, it is preferable that the gate insulation film be formed of the low-dielectric constant all over from just above the substrate to just below the gate electrode 106, at least at a portion over the source/drain region 107.

[0053] Each of FIGS. 6 to 10 shows the structure of a single transistor alone. However, needless to say, the structure of the above-described gate insulation film may be modified to cover cases where a plurality of transistors are formed, and the same advantageous effect can be obtained.

(Second Embodiment)

[0054] A MOS field-effect transistor according to a second embodiment of the present invention will now be described with reference to FIGS. 11A to 11D. In the second embodiment, as shown in FIG. 11A, the surface of the substrate is oxidized in an oxygen atmosphere at 700°C, following the step of FIG. 5B in the first embodiment. Thereby, a silicon oxide film 113 with a thickness of 1 nm is formed. Then, using a process such as CVD, a TiO_2 film 111 with a thickness of 15 nm is formed.

[0055] Subsequently, as shown in FIG. 11B, a polysilicon film with a thickness of 200 nm is deposited by LPCVD on the TiO_2 film 111. The polysilicon film is processed by anisotropic etching such as RIE and a gate electrode 106 is formed. Further, the TiO_2 film 111, too, is processed by anisotropic etching.

[0056] As is shown in FIG. 11C, using a process such as epitaxial growth, a silicon layer 114 is formed on a periphery of the gate electrode 106. In this case, since the silicon oxide film 113 is provided on the surface of the substrate, no silicon layer grows on the surface of the substrate and the silicon layer 114 can be selectively grown on the periphery of the gate electrode 106 alone.

[0057] As is shown in FIG. 11D, for example, As ions are implanted under conditions of 100 keV and 5.0×10^{15} cm^{-2}. The resultant structure is subjected to a heat treatment and source/drain regions 107 are formed.

[0058] Then, as shown in FIG. 11E, a silicon oxide film 109 with a thickness of 500 nm is deposited by CVD as an interlayer insulation film, following which contact holes 112 are opened by RIE on the source/drain regions 107 and gate electrode 106. At this time, the silicon oxide film 109 is made to fully extend under the silicon layer 114. The subsequent steps are common to those in the first embodiment.

[0059] In the second embodiment, too, such various modifications as have been described in connection with the first embodiment can be made, and the same advantageous effects can be obtained. In the second embodiment, the silicon layer 114 adjoining the gate electrode 106 is formed under the condition that facets are created. However, the silicon layer 114 may be formed such that no facets are created. In the case where the silicon layer 114 is formed under the condition that facets are created, the capacitance between the source/drain regions 107 and gate electrode 106 is made lower than in the case where no facets are created. Accordingly, it is more effective to form the silicon layer 114 under the condition that facets are created.

[0060] In the second embodiment, the gate electrode 106 is formed of a semiconductor and after it is processed, a semiconductor layer is formed to adjoin the gate electrode 106. However, there is no need to form both of them of semiconductors, and these may be formed of combinations of a semiconductor, a metal, a metal silicide, etc.

[0061] In the second embodiment, when the gate insulation film of the laminated structure is formed, the insulation film 113 provided immediately above the substrate is formed of a silicon oxide film. However, the insulation film 113 may be formed of some other kind of film, for instance, a silicon nitride film, an oxynitride film, or some other laminated insulation film. The method of forming the insulation film 113 provided immediately above the substrate is not limited to thermal oxidation, and it may be formed by a process such as deposition.

(Third Embodiment)

[0062] A MOS field-effect transistor according to a third embodiment of the present invention will now be described with reference to FIGS. 12A and 12B.

[0063] In the third embodiment, as is shown in FIG. 12A, a resist film 115 is formed on the substrate, following the step of FIG. 5E in the first embodiment. Part of the resist film 115 is selectively removed by a process such as photolithography.

[0064] Subsequently, as shown in FIG. 12B, the TiO_2 film 111 is subjected to isotropic etching such as CDE, and part of the TiO_2 film 111 on one of the source/drain regions 107 is removed. Thereafter, the resist film 115 is removed. The subsequent steps are common to the steps from the step of FIG. 5G in the first embodiment.

[0065] In the third embodiment, too, the dielectric constant of the gate insulation film between the gate electrode and source/drain can be lowered. In addition, such various modifications of the structure of the gate insulation film as have been described in connection with the first embodiment can be made, and the same advantageous effects can be obtained.

117 may form at or near the region from which the portion of the TiO_2 film 111 has been removed. Then, contact holes 112 are formed by RIE on the source/drain regions 107 and gate electrode 106. The subsequent steps are common to the steps in the first embodiment.

[0081] In the seventh embodiment, like the fifth embodiment, the void 117, which has a dielectric constant lower than that of silicon oxide, functions as the second gate insulation film. Thus, the short channel effect can be suppressed more effectively. In the seventh embodiment, too, such various modifications as have been described in connection with the first embodiment can be made, and the same advantageous effects can be obtained.

[0082] In the seventh embodiment, no void is created on that side of the gate insulation film, where the resist is applied at the time of subjecting the TiO_2 111 to isotropic etching. However, this is not essential, and the interlayer insulation film may be formed under the condition that voids may form on both sides of the gate insulation film.

[0083] As has been described above in detail, in the present invention, the dielectric constant of the gate insulation film in the region where the source/drain region overlaps the gate electrode is made lower than that of the gate insulation film on the channel region. Therefore, the short channel effect can be suppressed and the high current drive power obtained, while the parasitic capacitance can be reduced. As a result, a high-performance semiconductor device wherein the short channel effect is sufficiently suppressed and the high-speed operation is enabled can be realized.

Claims

1. A field-effect transistor characterized by comprising:

   a semiconductor substrate (101);
   a gate insulation film (111, 109', 109, 116) formed selectively on the semiconductor substrate (101);
   a gate electrode (106) formed on the gate insulation film;
   source/drain regions (107) formed in surface portions of the semiconductor substrate (101) along mutually opposed side surfaces of the gate electrode (106), the source/drain regions (107) having opposed end portions located immediately below the gate electrode (106), each of the opposed end portions having an overlapping region which overlaps the gate electrode (106); and
   a channel region (104) formed in a surface portion of the semiconductor substrate (101), which is sandwiched between the opposed source/drain regions (107),
   wherein that portion (109', 109, 116) of the gate insulation film (111, 109', 109, 116), which is located at the overlapping region where at least one of the source/drain regions (107) overlaps the gate electrode (106), has a lower dielectric constant than that portion (111) of the gate insulation film (111, 109', 109, 116), which is located on the channel region (104).

2. A field-effect transistor according to claim 1, characterized in that that portion (109', 109, 116) of the gate insulation film (111, 109', 109, 116), which has the lower dielectric constant, has a lower dielectric constant than that portion (111) of the gate insulation film (111, 109', 109, 116), which is located on the channel region (104), over an entire region in a film thickness direction of the gate insulation film.

3. A field-effect transistor according to claim 1, characterized in that that portion (111) of the gate insulation film (111, 109', 109, 116), which is located on the channel region (104), is formed of a first material, and at least a gate electrode end-side portion (109', 109, 116) of said overlapping region between at least one of the source/drain regions (107) and the gate electrode (106) is formed of a second material having a lower dielectric constant than the first material.

4. A field-effect transistor according to claim 3, characterized in that the first material forming that portion (111) of the gate insulation film (111, 109', 109, 116) which is located on the channel region (104) extends partially from on the channel region (104) to on the source/drain regions (107).

5. A field-effect transistor according to claim 3, characterized in that the first material contains at least one selected from the group consisting of a titanium oxide film, a silicon nitride film, a silicon oxynitride film, a tantalum pentoxide film, zirconium oxide film, hafnium oxide film, lanthanum oxide film, aluminum oxide film, yttrium oxide film and scandium oxide film.

6. A field effect transistor according to claim 3, characterized in that the first material contains a mixed film formed of at least two selected from the group consisting of titanium oxide, silicon nitride, silicon oxynitride, tantalum pentoxide, zirconium oxide, hafnium oxide, lanthanum oxide, aluminum oxide, yttrium oxide and scandium oxide.

7. A field-effect transistor characterized by comprising:

   a semiconductor substrate (101, 103);
   a gate electrode (106, 112) formed above the semiconductor substrate (101, 103);

hafnium oxide, lanthanum oxide, aluminum oxide, yttrium oxide and scandium oxide.

18. A method of fabricating a field-effect transistor, the method characterized by comprising the steps of:

forming a gate electrode (106) over a semiconductor substrate, with a gate insulation film (111) interposed therebetween;

forming a conductor film (114) selectively on a side surface of the gate electrode (106);

forming source/drain regions (107) in surface portions of the semiconductor substrate (103) in a self-alignment manner with the gate electrode (106) including the conductor film (114); and

forming a gate insulation region (109), which has a lower dielectric constant than the gate insulation film (111), at a region between the conductor film (114) and the substrate (103).

19. A method according to claim 18, characterized in that the step of forming the gate insulation region (109) with a lower dielectric constant than the gate insulation film (111) includes a step of forming, following the step of forming the conductor film (114) selectively on the side surface of the gate electrode (106), an interlayer insulation film (109) on the semiconductor substrate so as to cover the gate electrode (106), and filling a portion of the interlayer insulation film (109), as the gate insulation region, in the region between the conductor film (114) and the substrate (103).

20. A method according to claim 18, characterized in that the step of forming the gate insulation region with a lower dielectric constant than the gate insulation film (111) includes a step of forming, following the step of forming the conductor film (114) selectively on the side surface of the gate electrode (106), an interlayer insulation film (109) on the semiconductor substrate (103) so as to cover the gate electrode (106), the interlayer insulation film (109) forming a void (117) as the gate insulation region at a region among the gate insulation film (111), the conductor film (114) and the substrate (103).

21. A method according to claim 18, characterized in that the step of forming the conductor film (114) selectively on the side surface of the gate electrode (106) includes a step of growing a silicon layer (114) on the gate electrode (106) formed of polysilicon.

22. A method according to claim 18, characterized in that the step of forming the gate electrode (106) over the semiconductor substrate (103) with the gate insulation film (111) interposed therebetween includes a step of using, as material of the gate insulation film (111), at least one selected from the group consisting of a titanium oxide film, a silicon nitride film, a silicon oxynitride film and a tantalum pentoxide film.

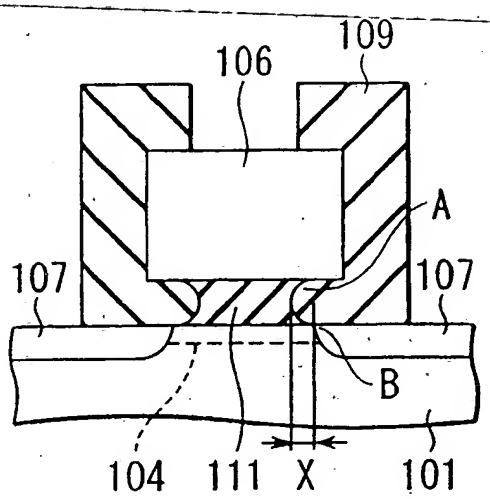

FIG. 6

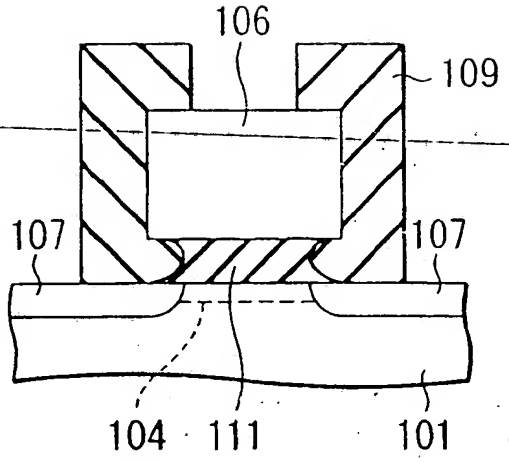

FIG. 8

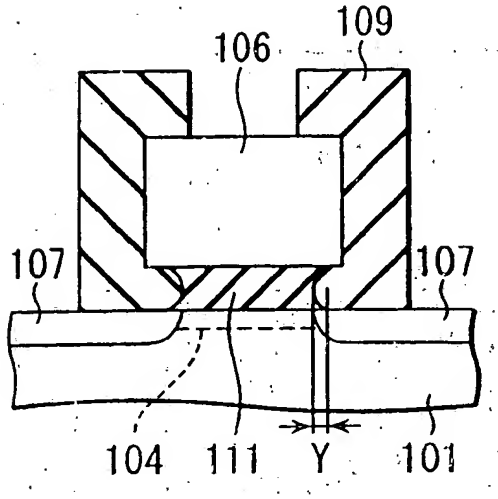

FIG. 7

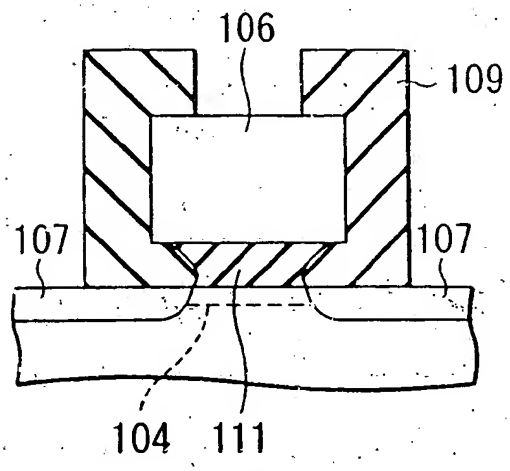

FIG. 9

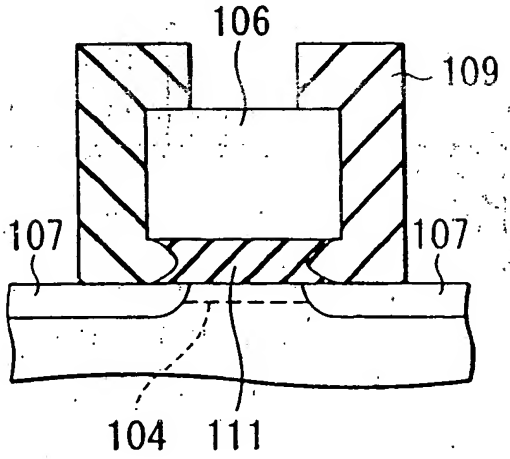

FIG. 10

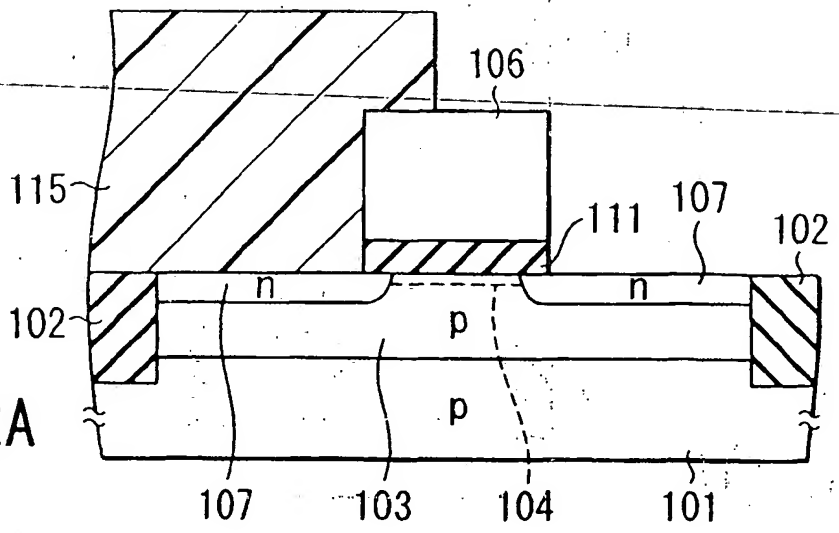

FIG. 12A

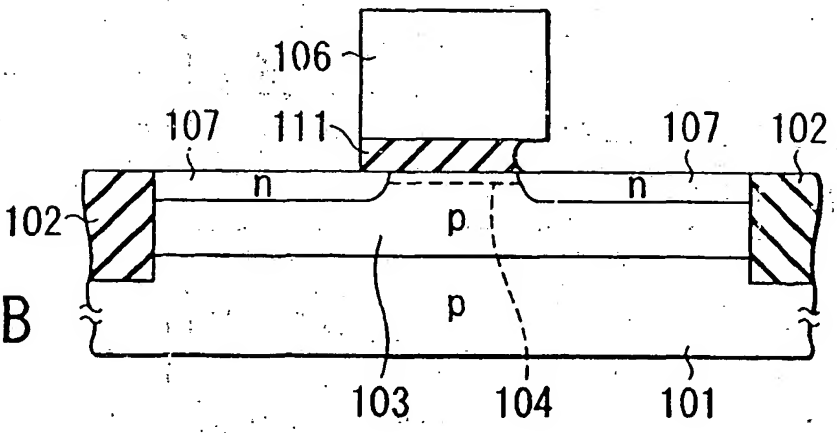

FIG. 12B

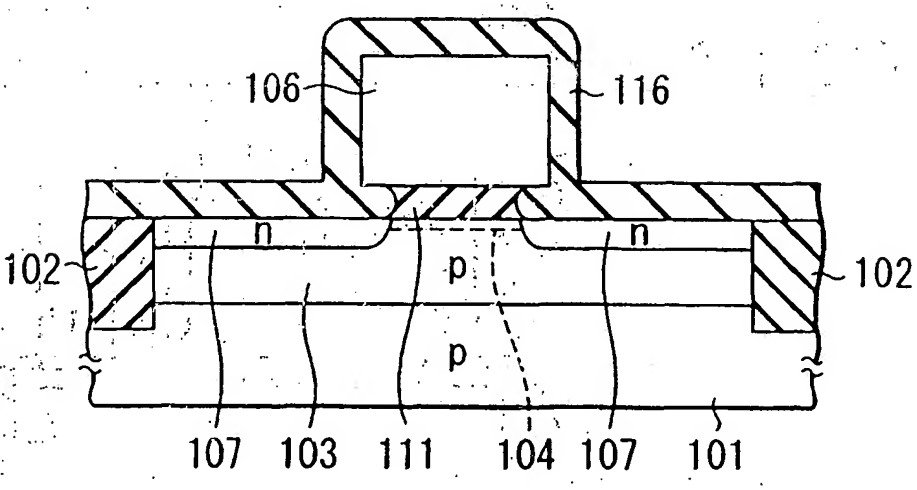

FIG. 13